REMARKS

The application has been reviewed in light of the final Office Action dated April 19, 2004. Claims 1-14 are pending and presented for reconsideration in this application, with claims 1 and 8 being in independent form.

Claims 1-7 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,638,530 to Pawate in view of U.S. Patent No. 6,088,785 to Hudson. Claims 8-14 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Japanese Patent Application No. JP01264034A to Nakajima et al. in view of Pawate and further view of Hudson.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that the pending claims are patentable over the cited art, for at least the following reasons.

This application relates to a digital signal processor (DSP) which has an internal memory for storing a program to be executed. DSP internal program memories are generally limited in capacity for assorted reasons. Therefore, programs required for digital signal processing, which tends to increase in complexity over time, are often stored on an external memory, and transferred to the internal memory in the DSP, as necessary.

Conventional program replacement approaches typically utilize a reset signal which is asserted when the program in the program memory is to be replaced, and then is removed to restart the DSP after program replacement is completed. In many instances, the program in the DSP internal memory must be replaced on the fly (for example, during modem communication). However, conventional program replacement techniques which require resetting the DSP (such as taught in Pawate) unacceptably incur an overhead for restarting program execution each time program replacement is performed.

Applicant devised program replacement techniques for DSPs which does not use a reset approach and can be used for on-the-fly program replacement. More specifically, Applicant found that programs can be expeditiously replaced by controlling a clock signal supplied to the internal memory of the DSP during program replacement, without requiring reinitialization of the digital signal processor.

Each of independent claims 1 and 8 includes this feature.

Pawate, as understood by Applicant, is directed to a smart card which acts as an interface between a host computer and any of various other external devices, such as a fax, a modem, a microphone, a speaker, etc. The smart card of Pawate has a DSP 170 onboard. A shared memory consisting of common memory 150 and attribute memory 160, which are both **external** to the DSP, can be accessed by the host computer as well as by the DSP. In addition, the DSP has its own memory which stores a program to be executed by the DSP. The shared memory serves data storage and program storage for supporting paging of the DSP's memory. Paging by the DSP memory from the shared memory is performed only when the DSP is active and executing instructions (in smart mode), that is, while the clock signal is actively supplied to the DSP.

According to Pawate, the host computer can load a desired program into the memory of the DSP and then initialize the DSP (see Pawate, column 13, line 66 through column 14, lines 2). After the DSP has thus been initialized, the host computer can then control the clock of the DSP to place the DSP into a power-saving mode while the host computer accesses other functional portions of the smart card.

While Pawate suggests controlling the clock of the DSP to place the DSP into a power saving mode which allows the host computer to access the shared memory (external to the DSP), Pawate simply does not disclose or suggest controlling outputting of the clock signal to the

digital signal processor so that programs stored in the external memory part can be forwarded to the internal memory part, as provided by the claimed invention.

Hudson does not cure the deficiencies of Pawate.

Hudson, as understood by Applicant, is directed to an signal processing system which is adaptable for performing any of various signal processing functions. The system includes a signal processing subsystem 114 and a memory pool 116 which can be packaged as separate devices or as a single package. The subsystem is coupled to the memory pool, and can be configured to perform a particular signal processing function by loading appropriate function-defining code from the memory pool into local memory.

The Office Action cites Hudson as purportedly disclosing (a) control of output of a signal without initialization of the DSP, and (b) utilizing a lower frequency clock to place a subsystems into low power mode and halt mode which allows the subsystem to operate at a lower frequency.

While Hudson discloses a unit 366 which controls clock generation and power management, Hudson, like Pawate, does not teach or suggest, however, controlling outputting of the clock signal to the digital signal processor so that programs stored in the external memory part can be forwarded to the internal memory part, as provided by the claimed invention.

Thus, even the combination of Pawate and Hudson does not disclose or suggest each and every feature of the claimed invention, and therefore Pawate and Hudson do not render the claimed invention unpatentable.

Nakajima was cited against claims 8-14 as purportedly showing use of a modem for modulating/demodulating communication data by using a signal processing apparatus which comprises a DSP. The Office Action acknowledges, however, that Nakajima does not disclose or suggest controlling outputting of the clock signal to the digital signal processor so that programs

stored in the external memory part can be forwarded to the internal memory part, as provided by the claimed invention.

In short, Applicant simply does not find teaching or suggestion in the cited art of controlling outputting of the clock signal to the digital signal processor so that programs stored in the external memory part can be forwarded to the internal memory part, as provided by the claimed invention. As noted above, the paging operation of Pawate can be performed only when the DSP is active, that is, when a clock signal is being actively supplied to the DSP.

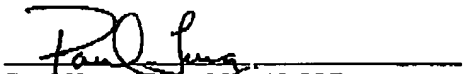
Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1 and 8, and the claims depending therefrom, are patentable over the cited references.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125. The Office is hereby authorized to charge any additional fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,



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